

Saed Thaher

Cambridge, MA · saedth@mit.edu · linkedin.com/in/saed-thaher

Hardware engineering: ASIC / RTL design, digital IC design, FPGA and computer architecture

EDUCATION

Massachusetts Institute of Technology — Expected May 2028

B.S. in Electrical Engineering with Computing (Course 6-5) · GPA 4.5 / 5.0

- Coursework: Analysis and Design of Digital Integrated Circuits (6.6010), Digital Systems Laboratory (6.205), Computation Structures, Nanoelectronics and Computing Systems, Algorithms, Linear Algebra, Introduction to Machine Learning, Electrical Circuits

EXPERIENCE

MIT STAR Lab · Undergraduate Researcher (UROP) — Aug 2026 – Present

Cambridge, MA · Advisor: Prof. Kerri Cahoy

- Architecting clocking, reset, and AXI/NoC interconnect for a Versal AI Edge SOM platform supporting the CIPS and programmable logic domains for an onboard CubeSat compute system
- Deploying an INT8-quantized ResNet18 CNN onto the Versal AI Engine array for onboard image classification under strict downlink bandwidth constraints; 98/100 accuracy on a labelled test set at 11 ms per image
- Evaluating boot-time and power tradeoffs across configurations, achieving a 5-second boot target within a 36W power budget
- Building and validating hardware bring-up over JTAG and UART, debugging platform-level integration issues across the Vivado/Vitis toolchain; root-caused two faults that had kept the accelerator from running

A*STAR Institute of Microelectronics (IME) · FPGA Engineering Intern

Jun 2026 – Jul 2026
Singapore · MISTI Program

- Designed a bubble error correction scheme for a time-to-digital converter (TDC), improving linearity in a high-resolution timing measurement system
- Built a Python-based DNL/INL simulation framework to characterize TDC nonlinearity, reducing measured error by 57% after correction
- Implemented and verified three candidate TDC architectures through testbench-driven RTL verification, Genus synthesis, and Xcelium simulation

MIT Department of EECS · Lab Assistant, 6.101 Fundamentals of Programming

Feb 2026 – May 2026
Cambridge, MA

- Held office hours and debugging sessions for 100+ students on Python fundamentals, recursion, and data structures

UCLouvain · Electrical Engineering Research Intern — May 2025 – Jul 2025

Louvain-la-Neuve, Belgium · MISTI Program

- Developed a coupled thermal-electrical COMSOL model to characterize heat dissipation in a power electronics test setup

PROJECTS

RISC-V CPU Design · 6.1910 Computation Structures — Oct 2025 – Dec 2025

- Designed a 4-stage pipelined RISC-V CPU in Minispec with caches, hazard detection and forwarding logic
- Added a custom 4×INT8 packed-multiply instruction (packmul); cut MNIST inference from 24.6 ms to 0.77 ms (32×) for 7.7% more logic area

FPGA Video and Memory Systems · 6.205 Digital Systems Laboratory

Sep 2026 – Nov 2026

- Built a 720p HDMI pipeline in SystemVerilog on a Spartan-7 (TMDS encoding, 371.25 MHz serializer), a camera frame buffer, and real-time 3×3 convolution with timing met
- Implemented a DDR3 frame buffer across three clock domains using asynchronous FIFOs and a Wishbone memory controller

Gesture-Controlled Synthesizer · 6.205 final project

Nov 2026 – Present

- Designing a polyphonic additive synthesis engine and audio output on an FPGA, time-multiplexing one datapath across all voices (team of three)

LEADERSHIP

MIT Model United Nations

Cambridge, MA

Chief Financial Officer, Executive Board · Committee Co-Chair

Delta Psi Fraternity

Cambridge, MA

Alumni Relations Secretary

SKILLS

- **Programming:** Python, C, Assembly
- **Digital design and verification:** Verilog, SystemVerilog, RTL design and implementation, digital logic design, testbench-driven verification, PCB design, SPICE simulation
- **EDA tools:** Cadence Virtuoso, Spectre, Calibre (DRC/LVS), Cadence Xcelium, Cadence Genus, Xilinx Vivado, PetaLinux, KiCad, SolidWorks, COMSOL
- **Semiconductor fundamentals:** CMOS device physics, design for manufacturing
- **Lab:** oscilloscope, multimeter, logic analyzer, Linux
- **Languages:** Arabic (native), English (bilingual), French (intermediate)